

1 7 The method of claim 4 further comprising filtering the
data receive count and the data complete count, the data
resampling being a function of the filtered counts.

5 8. The method of claim 7 further comprising subtracting
said filtered data receive count and said filtered data complete
count, the data resampling being a function of the difference
between counts.

10 9. The method of claim 8 wherein the fractional resampling
comprises upsampling the data if the data received count exceeds
the data complete count and downsampling the data if the data
complete count exceeds the data received count.

15 10. The method of claim 4 further comprising generating a
third clock, wherein the date receive count and data complete
clock count comprises incrementing the count using the third
clock.

20 11. A synchronization circuit, comprising:
 an error generation unit that generates a clock error signal
as a function of an average far end sampling rate and a near end
sampling rate; and
 a sample tracker adapted to receive sampled data packets,
25 wherein the sample tracker fractionally resamples the sampled
data as a function of the clock error signal.

30 12. The synchronization circuit of claim 11 wherein said
error generation unit comprises one or more counters incremented
by a local reference clock, a first latch adapted to store count
of at least a portion of a cycle between packet arrivals, a
second latch adapted to store at least a portion of a cycle
between packet completions, wherein said clock error signal is
a function of ratio of packet arrival count and packet completion
35 count.

1 13. The synchronization circuit of claim 12 wherein the
sample tracker upsamples the data if the packet arrival count
exceeds the packet completion count and downsamples the data if
the packet completion count exceeds the packet arrival count.

5 14. The synchronization circuit of claim 12 further
comprising a filter between the first latch and the sample
tracker for averaging transition between different sampling
rates.

10 15. The synchronization circuit of claim 14 wherein the
filter is a single pole, low pass filter.

15 16. The synchronization circuit of claim 12 further
comprising a digital-to-analog converter to convert the
fractionally resampled data to an analog voice signal.

20 17. The synchronization circuit of claim 12 further
comprising a processor to activate the first latch each time a
packet of sampled data is received.

25 18. A network gateway adapted to exchange voice signals
between a network line at a first clock frequency and a packet
based network at a second clock frequency, comprising:

 a network port to interface with a packet based network;
 a telephony port to interface with a telephony device;
 a processor coupled to each of the ports; and

30 a voice synchronizer, coupled between said network and
telephony ports, comprising an error generation unit for
generating a clock error signal in accordance with ratio of said
first and second clocks and a sample tracker, adapted to receive
data packets, wherein the sample tracker fractionally resamples
the received data as a function of the clock error signal.

1 19. The network gateway of claim 18 further comprising a
transceiver coupled between the processor and the network port.

5 20. The network gateway of claim 19 wherein the transceiver
comprises a media access controller (MAC) coupled to the
processor, and a modulator and a demodulator both disposed
between the MAC and the network port.

10 21. The network gateway of claim 18 further comprising a
voice circuit coupled between the telephony port and the
processor.

15 22. The network gateway of claim 21 wherein the voice
circuit formats voice signals flowing from the telephony port to
the processor into voice signal packets, and formats voice
signals flowing from the processor to the telephony port into a
telephony format.

20 23. The network gateway of claim 22 wherein the telephony
format comprises pulse code modulation.

25 24. The network gateway of claim 18 wherein said error
generation unit comprises one or more counters incremented by a
local reference clock, a first latch adapted to store count of
at least a portion of a cycle between packet arrivals, a second
latch adapted to store at least a portion of a cycle between
packet completions, wherein said clock error signal is a function
of ratio of packet arrival count and packet completion count.

30 25. The network gateway of claim 24 wherein the sample
tracker upsamples the data if the packet arrival count exceeds
the packet completion count and downsamples the data if the
packet completion count exceeds the packet arrival count .

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1 26. The network gateway of claim 24 further comprising a
filter between the first latch and the sample tracker for
averaging transition between different sampling rates.

5 27. The network gateway of claim 26 wherein the filter is
a single pole, low pass filter.

10 28. The network gateway of claim 24 further comprising a
digital-to-analog converter to convert the fractionally resampled
data to an analog voice signal.

15 29. The network gateway of claim 24 further comprising a
processor to activate the first latch each time a packet of
sampled data is received.